Par4All: Auto-Parallelizing C and Fortran for the CUDA Architecture

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10/1/2009
http://www.par4all.org
Through its Wild Systems subsidiary company

- **WildNode hardware desktop accelerator**
  - Low noise for in-office operation
  - x86 manycore
  - nVidia Tesla GPU Computing
  - Linux & Windows

- **WildHive**
  - Aggregate 2-4 nodes with 2 possible memory views
    - Distributed memory with Ethernet or InfiniBand
    - Virtual shared memory through Linux Kerrighed for single-image system

http://www.wild-systems.com
HPC Project software and services

- Parallelize and optimize customer applications, co-branded as a bundle product in a WildNode (e.g. Presagis Stage battle-field simulator)
- Acceleration software for the WildNode
  - GPU-accelerated libraries for Matlab/Octave/R
  - Transparent execution of Matlab on the WildNode
- Remote display software for Windows on the WildNode

HPC consulting

- Optimization and parallelization of applications
- High Performance?... not only TOP500-class systems: power-efficiency, embedded systems, green computing...
- Embedded system and application design
- Training in parallel programming (OpenMP, MPI, TBB, CUDA, OpenCL...)

Par4All in CUDA — GPU conference 10/1/2009
We need software tools

- HPC Project needs tools for its hardware accelerators (*Wild Nodes* from *Wild Systems*) and to parallelize, port & optimize customer applications
- Application development: long-term business ~ long-term commitment in a tool that needs to survive to (too fast) technology change
- Unreasonable to begin yet another new compiler project...
- Many academic Open Source projects are available...
- ...But customers need products 😁

**Par4All**

- ~ Funding an initiative to industrialize Open Source tools
- PIPS is the first project to enter the Par4All initiative

http://www.par4all.org
Outline

1. Par4All
2. CUDA generation
3. Results
4. Conclusion
Hardware is moving quite (too) fast but...

What has survived for 50+ years?
Fortran programs...

What has survived for 30+ years?
C programs...

- A lot of legacy code could be pushed onto parallel hardware (accelerators) with automatic tools...
- Not as efficient as hand-tuned programs, but quick production phase
- Need automatic tools for source-to-source transformation to leverage existing software tools for a given hardware
• PIPS (Interprocedural Parallelizer of Scientific Programs): Open Source project from Mines ParisTech... ≈ 150 hy, 21-year old!
• Funded by many people (French DoD, Industry & Research Departments, University, CEA, IFP, Onera, ANR (French NSF), European projects, regional research clusters...)
• Project that coined polytope model-based compilation
• ≈ 456 KLOC according to David A. Wheeler’s SLOCCount
• ... but modular and sensible approach to pass through the years
  ▶ ≈300 phases (parsers, analyzers, transformations, optimizers, parallelizers, code generators, pretty-printers...) that can be combined for the right purpose
  ▶ NewGen object description language for language-agnostic automatic generation of methods, persistence, object introspection, visitors, accessors, constructors, XML marshaling for interfacing with external tools...
Interprocedural à la make engine to chain the phases as needed. Lazy construction of resources.

Polytope lattice (linear algebra) used for semantics analysis, transformations, code generation... to deal with big programs, not only loop-nests.

Huge on-going efforts to industrialize the project, extension of the semantics analysis for C.

Around 15 programmers currently developing in PIPS (Mines ParisTech, HPC Project, IT SudParis, TÉLÉCOM Bretagne, RPI) with public svn, Trac, mailing lists, IRC, Plone, Skype... and use it for many projects.

But still...

Huge need of documentation (even if PIPS uses literate programming...)

Need of industrialization

Need further communication to increase community size

Par4All initiative
Current PIPS usage

- Automatic parallelization (C & Fortran to OpenMP)
- Distributed memory computing with OpenMP-to-MPI translation (STEP project)
- Generic vectorization for SIMD instructions (SSE, VMX...) (SAC project)
- Parallelization for embedded systems (SCALOPES)
- Compilation for hardware accelerators (Ter@PIX, SPoC, SIMD, FPGA...)
- High-level hardware accelerators synthesis generation for FPGA
- Reverse engineering & decompiler (reconstruction from binary to C)

Logical next stop

GPU! 😊
Current PIPS usage

- Automatic parallelization (C & Fortran to OpenMP)
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Logical next stop

GPU! 😊
A sequential program on a host launches computational-intensive kernels on a GPU

- Allocate storage on the GPU
- Copy-in data from the host to the GPU
- Launch the kernel on the GPU
- Copy-out the results from the GPU to the host
- Deallocate the storage on the GPU
Challenges in automatic CUDA generation

- Find parallel kernels
- Improve data reuse inside kernels to have better compute intensity (even if the memory bandwidth is quite higher than on a CPU...)
- Access the memory in a GPU-friendly way (to coalesce memory accesses)
- Take advantage of complex memory hierarchy that make the GPU fast (shared memory, cached texture memory, registers...)
- Reduce the copy-in and copy-out transfers that pile up on the PCIe
- Reduce memory usage in the GPU (no swap there, yet...)
- Limit inter-block synchronizations
- Overlap computations and GPU-CPU transfers (via streams)
Automatic parallelization

Most fundamental for a parallel execution
Finding parallelism!

Several parallelization algorithms are available in PIPS

- For example classical Allen & Kennedy use loop distribution more vector-oriented than kernel-oriented \(\uparrow\) (or need later loop-fusion)
- Coarse grain parallelization based on the independence of array regions used by different loop iterations
  - Currently used because generates GPU-friendly coarse-grain parallelism
  - Accept complex control code without *if-conversion*
Parallel code $\leadsto$ Kernel code on GPU

- Need to extract parallel source code into kernel source code: outlining of parallel loop-nests

- Before:

```c
for (i = 1; i <= 499; i++)
    for (j = 1; j <= 499; j++) {
        save[i][j] = 0.25*(space[i - 1][j] + space[i + 1][j] + space[i][j - 1] + space[i][j + 1]);
    }
```
After:

```c
p4a_kernel_launcher_0(space, save);
[...]
void p4a_kernel_launcher_0(float_t space[SIZE][SIZE],
                          float_t save[SIZE][SIZE]) {
    for (i = 1; i <= 499; i += 1)
        for (j = 1; j <= 499; j += 1)
            p4a_kernel_0(i, j, save, space);
}
[...]
void p4a_kernel_0(float_t space[SIZE][SIZE],
                   float_t save[SIZE][SIZE],
                   int i,
                   int j) {
    save[i][j] = 0.25*(space[i-1][j]+space[i+1][j]
                      +space[i][j-1]+space[i][j+1]);
}
```
Memory accesses are summed up for each statement as *regions* for array accesses: integer polytope lattice.

There are regions for write access and regions for read access.

The regions can be *exact* if PIPS can prove that only these points are accessed, or they can be *inexact*, if PIPS can only find an over-approximation of what is really accessed.
From array regions to GPU memory allocation

Example

```c
for (i = 0; i <= n-1; i += 1)
    for (j = i; j <= n-1; j += 1)
        h_A[i][j] = 1;
```

can be decorated by PIPS with write array regions as:

```c
// <h_A[PHI1][PHI2]--W-EXACT--{0<=PHI1, PHI2+1<=n, PHI1<=PHI2}>
for (i = 0; i <= n-1; i += 1)

// <h_A[PHI1][PHI2]--W-EXACT--{PHI1==i, i<=PHI2, PHI2+1<=n, 0<=i}>
for (j = i; j <= n-1; j += 1)

// <h_A[PHI1][PHI2]--W-EXACT--{PHI1==i, PHI2==j, 0<=i, i<=j, 1+j<=n}>
    h_A[i][j] = 1;
```

- These read/write regions for a kernel are used to allocate with a `cudaMalloc()` in the host code the memory used inside a kernel and to deallocate it later with a `cudaFree()`
Conservative approach to generate communications

- Associate any GPU memory allocation with a copy-in to keep its value in sync with the host code.
- Associate any GPU memory deallocation with a copy-out to keep the host code in sync with the updated values on the GPU.
- But a kernel could initialize an array, or use the initial values without writing into it, or use it as a local (private) array.
- (PIPS does have many privatization phases)
• PIPS gives 2 very interesting region types for this purpose
  - **In-region** abstracts what really needed by a statement
  - **Out-region** abstracts what really produced by a statement to be used later elsewhere

• In-Out regions can directly be translated with CUDA into
  - **copy-in**
    ```c
    cudaMemcpy(accel_address, host_address, size, cudaMemcpyHostToDevice)
    ```
  - **copy-out**
    ```c
    cudaMemcpy(host_address, accel_address, size, cudaMemcpyDeviceToHost)
    ```
Loop normalization

- Hardware accelerators use fixed iteration space (CUDA: thread index starting from 0...)
- Parallel loops: more general iteration space
- Loop normalization

**Before**

```c
for (i = 1; i < SIZE - 1; i++)
    for (j = 1; j < SIZE - 1; j++) {
        save[i][j] = 0.25*(space[i - 1][j] + space[i + 1][j]
                           + space[i][j - 1] + space[i][j + 1]);
    }
```

**After**

```c
for (i = 0; i < SIZE - 2; i++)
    for (j = 0; j < SIZE - 2; j++) {
        save[i + 1][j + 1] = 0.25*(space[i][j + 1] + space[i + 2][j + 1]
                                   + space[i + 1][j] + space[i + 1][j + 2]);
    }
```
Parallel loop nests are compiled into a CUDA kernel wrapper launch

The kernel wrapper itself gets its virtual processor index with some blockIdx.x*blockDim.x + threadIdx.x

Since only full blocks of threads are executed, if the number of iterations in a given dimension is not a multiple of the blockDim, there are incomplete blocks

An incomplete block means that some index overrun occurs if all the threads of the block are executed
From preconditions to iteration clamping

- So we need to generate code such as

```c
void p4a_kernel_wrapper_0(int k, int l,...)
{
    k = blockIdx.x*blockDim.x + threadIdx.x;
    l = blockIdx.y*blockDim.y + threadIdx.y;
    if (k >= 0 && k <= M - 1 && l >= 0 && l <= M - 1)
        kernel(k, l, ...);
}
```

But how to insert these guards?

- The good news is that PIPS owns preconditions that are predicates on integer variables. Preconditions at entry of the kernel are:

```c
// P(i, j, k, l) {0 <= k, k <= 63, 0 <= l, l <= 63}
```

- Guard ≡ directly translation in C of preconditions on loop indices that are GPU thread indices
• Launching a GPU kernel is expensive
  ► so we need to launch only kernels with a significant speed-up
    (launching overhead, memory CPU-GPU copy overhead...)

• Some systems use \#pragma to give a go/no-go information to parallel execution

\begin{verbatim}
#pragma omp parallel if(size>100)
\end{verbatim}

• ∃ phase in PIPS to symbolically estimate complexity of statements

• Based on preconditions

• Use a SuperSparc2 model from the ’90s... 😊

• Can be changed, but precise enough to have a coarse go/no-go information

• To be refined: use memory usage complexity to have information about memory reuse (even a big kernel could be more efficient on a CPU if there is a good cache use)
- Reduction are common patterns that need special care to be correctly parallelized
- Reduction detection already implemented in PIPS
- Efficient computation in CUDA needs to create local reduction trees in the thread-blocks
- On-going implementation at Rensselaer Polytechnic Institute (RPI) with parallel-prefix
Fortran to CUDA

- Fortran 77 parser available in PIPS
- CUDA is C/C++ with some restrictions on the GPU-executed parts
- Need a Fortran to C translator (f2c...)?
- Only one internal representation is used in PIPS
  - Use the Fortran parser
  - Use the C pretty-printer
- But the IO Fortran library is complex to use... and to translate
  - If you have IO instructions in a Fortran loop-nest, it is not parallelized anyway because of sequential side effects 😊
  - So keep the Fortran output everywhere but in the parallel CUDA kernels
  - Apply a memory access transposition phase $a(i,j) \rightarrow a[j-1][j-1]$ inside the kernels to be pretty-printed as C
- We could output CUDA Fortran directly when available
Fortran to CUDA

- Fortran 90 and 95 support is quite interesting
  - Dynamic allocation
    - Avoid nasty user allocation functions in Fortran 77 used to allocate objects in a big array...
    - 🚸 Was a parallelism killer...
  - Derived types (C structures)
    - Avoid using more dimensions to arrays to simulate structure fields in Fortran 77
    - 🚸 Was a parallelism killer, used useless dereferencing...
  - Pointers
    - Useful to navigate through recursive derived type
    - 🚸 Was a parallelism killer, used useless dereferencing...
    - 🍀 Mmm... Try to avoid this anyway 🙃

- Most of these concepts are in C, so are already dealt by PIPS
- ➔ On-going Fortran 95 support with the `gfortran` parser from GCC

Par4All in CUDA — GPU conference 10/1/2009
HPC Project, Mines ParisTech, TÉLÉCOM Bretagne, RPI
Ronan Keryell et al.

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- Object-oriented Fortran 2003? Hard for a compiler to understand the object-oriented interprocedural polymorphism...
- Programmer should avoid it at low-level for performance issues
  - Some high-performance optimizations need to change data organization...
  - ... that means object model restructuring 😊
- Is there a cultural community big enough to have object-oriented Fortran programs? Need a big library ecosystem to have competitive advantage...
CUDA can not be directly represented in the internal representation (IR, abstract syntax tree) such as \texttt\{\_\_device\_\} or \texttt{<<< >>>}

PIPS motto: keep the IR as simple as possible

Use some calls to intrinsics functions that can be represented directly

Intrinsics functions are implemented with (macro-)functions

- \texttt{p4a_accel.h} has indeed currently 2 implementations
  - \texttt{p4a_accel-CUDA.h} than can be compiled with CUDA for nVidia GPU execution or emulation on CPU
  - \texttt{p4a_accel-OpenMP.h} that can be compiled with an OpenMP compiler for simulation on a (multicore) CPU
```c
int main(int argc, char *argv[]) {
    [...]

    float_t (*p4a_var_space)[SIZE][SIZE];
    P4A_ACCEL_MALLOC(&p4a_var_space, sizeof(space));
    P4A_COPY_TO_ACCEL(space, p4a_var_space, sizeof(space));

    float_t (*p4a_var_save)[SIZE][SIZE];
    P4A_ACCEL_MALLOC(&p4a_var_save, sizeof(save));
    P4A_COPY_TO_ACCEL(save, p4a_var_save, sizeof(save));

    P4A_ACCEL_TIMER_START;

    for(t = 0; t < T; t++)
        compute(*p4a_var_space, *p4a_var_save);

    double execution_time = P4A_ACCEL_TIMER_STOP_AND_FLOAT_MEASURE();
    P4A_COPY_FROM_ACCEL(space, p4a_var_space, sizeof(space));

    P4A_ACCEL_FREE(p4a_var_space);
    P4A_ACCEL_FREE(p4a_var_save);
```
void compute(float_t space[SIZE][SIZE],
          float_t save[SIZE][SIZE]) {

    p4a_kernel_launcher_0(space, save);

    void p4a_kernel_launcher_0(float_t space[SIZE][SIZE],
                                float_t save[SIZE][SIZE]) {

        P4A_CALL_ACCEL_KERNEL_2D(p4a_kernel_wrapper_0, SIZE, SIZE,
                                 space, save);

    }

    P4A_ACCEL_KERNEL_WRAPPER void

    p4a_kernel_wrapper_0(float_t space[SIZE][SIZE],
                         float_t save[SIZE][SIZE]) {

        int j;
        int i;

        i = P4A_vp_0;
        j = P4A_vp_1;
if (i >= 1 && i <= SIZE - 1 && j >= 1 && j <= SIZE - 1)
    p4a_kernel_0(space, save, i, j);
}

P4A_ACCEL_KERNEL void p4a_kernel_0(float_t space[SIZE][SIZE],
                                   float_t save[SIZE][SIZE],
                                   int i,
                                   int j) {
    save[i][j] = 0.25*(space[i-1][j]+space[i+1][j]
                       +space[i][j-1]+space[i][j+1]);
}
Outline

1. Par4All
2. CUDA generation
3. Results
4. Conclusion
Results on a customer application

- Holotetrix’s primary activities are the design, fabrication and commercialization of prototype diffractive optical elements (DOE) and micro-optics for diverse industrial applications such as LED illumination, laser beam shaping, wavefront analyzers, etc.
- Hologram verification with direct Fresnel simulation
- Program in C
- Parallelized with
  - Par4All CUDA and CUDA 2.3, Linux Ubuntu x86-64
  - Par4All OpenMP, gcc 4.3, Linux Ubuntu x86-64
- Reference: Intel Core2 6600 @ 2.40GHz

http://www.holotetrix.com

Visit us at the Wild Systems booth #35 for a demo
Comparative performance

![Graph showing comparative performance of different hardware configurations.](image)

- **2c Intel 6600 2.4 GHz (OpenMP)**
- **8c Intel X5472 3 GHz (OpenMP)**
- **8c X5570 2.9 GHz (OpenMP)**
- **1c Intel 6600 2.4 GHz**
- **1c Intel X5472 3 GHz**
- **or X5570 2.9 GHz**

Matrix size (Kbytes)

- **GTX 200 192 streams**
- **Tesla 1060 240 streams**

**DOUBLE PRECISION**

Average time in s (5 samples)
Comparative performance

- Tesla 1060 240 streams
- GTX 200 192 streams
- 8c Intel X5472 3 GHz (OpenMP)
- 2c Intel Core2 6600 2,4 GHz (OpenMP)
- 1c Intel X5472 3 GHz

Speed up vs Matrix size (Kbytes)

Reference 1c Intel 6600 2,4 GHz

DOUBLE PRECISION
Results

Keep it simple (precision)

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<thead>
<tr>
<th>Matrix size (Kbytes)</th>
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SIMPLE PRECISION

Quadro FX 3700M (G92GL) 128 streams
GTX 200 192 streams
Tesla 1060 240 streams
**Results**

Keep it simple (precision)

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**SIMPLE PRECISION**
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Take advantage of C99

- **BaC99k to C99imple C99ings**
- **Avoiding using C99umbersome old C C99onstruC99ts C99an lead to C99leaner C99ode, more effiC99ient and more parallelizable C99ode with Par4All**
- **C99 adds C99ympaC99etiC99 features that are unfortunately not well known:**
  - **MultidimenC99ional arrays with non-statiC99c size**
    - Avoid `malloc()` and useless pointer C99onstruC99ions
    - You C99an have arrays with a dynamiC99 size in funC99tion parameters (as in Fortran)
    - Avoid useless linearizing C99omputaC99ions (a[i][j] instead of a[i+n*j]...)
    - Avoid most of `alloca()`
  - **TLS (Thread-Local Storage) ExtenC99ion C99an express independent storage**
  - **C99omplex numbers and booleans avoid further struC99tures or enums**
Why open source?

- Once upon a time, a research team in Luxembourg decided to experiment program transformations with genetic algorithms...
- Main idea:
  - Represent the transformations applied to a program as a gene
  - Make the genes to evolve
  - Measure the performance
  - Select and iterate
- They used PIPS to implement this
- Side effects
  - Now PIPS is scriptable in Python (PYPS)
  - Algorithm written in Python
  - We have an automated way to try many different optimizations to generate better CUDA kernels!

Stay tuned...
Conclusion

Future work

- Use advanced tiling to take advantage of shared memory and texture cache
- Select optimal transformations and code generation parameter by using genetic algorithm system already in PIPS
- Using complexity information to select the best execution mode (GPU or CPU)
- Mix GPU and CPU execution, with SSE\textsubscript{x}, OpenMP and/or MPI
- Matlab to CUDA compiler
- OpenCL support via OpenGPU project
- Eclipse (EcliPIPS) integration via OpenGPU project
- If someone spent some time to write \#pragma information... Use them! 😊
- Generate run-time specialization and speculation when some static information is lacking at compilation time
Future work

- We have already PhD students, engineers and researchers around Par4All, but many hard issues remains, so we need you too... 😊
Conclusion

- GPU (and other heterogeneous accelerators): impressive peak performances and memory bandwidth, power efficient
- Looks like to the 80’s: many accelerators, vectors, parallel computers
  - Need to port the programs to new architectures
  - Many start-ups
- ...but some hypothesis changed, hardware constraints \(\Rightarrow\) we can no longer escape parallelism! No longer a niche market!
- Programming is *quite more* complex... 😞
- Non-functional specifications (speed, time, power, parallelism...) not taken into account by main-stream programming environment and teaching (high-level object programming...)
- And programs are quite bigger now! 😞
- Application source code evolves slowly compared to hardware
Conclusion

- Capitalize on this with a source-to-source tool!
- Before addressing parallelism, may be interesting to optimize the sequential program (algorithmic, coding, right tools...)
- Take a positive attitude...Parallelization is a good opportunity for deep cleaning (refactoring, modernization...) ~ improve also the original code
- A cleaner code is often easier to parallelize automatically or manually
- Do not forget simple precision exist too... 😊
- 🚫 Entry cost
- 🚫 🚫 🚫 Exit cost! 😊
- Par4All initiative aims at minimizing entry cost and exit cost
  - Use source-to-source compilers to surf on the best back-ends (CUDA for nVidia GPU)
  - Avoid manual work with preprocessing, tools, code generators...
Open source architecture to collaborate with best research teams
Use standards and Open Source for long-term investment
Open source to avoid sticking to a one-company solution
Hide manual work in preprocessing, tools, code generators...
Can accept \#pragma from other products as a second-source
Come on and participate to the initiative!

You are not a compiler developer and you may ask what to keep from such a talk?

If you understand better how a compiler work, you can write code that fits better the compiler... 😊

Visit us at the Wild Systems booth #35 for a demo
Par4All is currently supported by...

- HPC Project
- Mines ParisTech
- Institut TÉLÉCOM/TÉLÉCOM Bretagne
- Rensselaer Polytechnic Institute
- European ARTEMIS SCALOPES project
- French NSF (ANR) FREIA project
- French Images and Networks research cluster TransMedi@ project
- French System@TIC research cluster OpenGPU project
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