

Fast Tridiagonal Solvers on GPU

Yao Zhang
John Owens
UC Davis

Jonathan Cohen
NVIDIA

GPU Technology Conference 2009

Outline

- Introduction
- Algorithms
 - Design algorithms for GPU architecture
- Performance
 - Bottleneck-based vs. Component-based performance model
- Summary

What is it used for?

- Scientific and engineering computing
 - Alternating direction implicit (ADI) methods
 - Numerical ocean models
 - Semi-coarsening for multi-grid solvers
 - Spectral Poisson Solvers
 - Cubic Spline Approximation
- Video games and computer-animated films
 - Depth of field blurs
 - Fluid simulation

A Classic Serial Algorithm

- Gaussian elimination in tridiagonal case (Thomas algorithm)

$$\begin{pmatrix} 1 & c'_1 & & & \\ 0 & 1 & c'_2 & & \\ & 0 & 1 & c'_3 & \\ & & 0 & 1 & c'_4 \\ & & & 0 & 1 \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{pmatrix} = \begin{pmatrix} d'_1 \\ d'_2 \\ d'_3 \\ d'_4 \\ d'_5 \end{pmatrix}$$

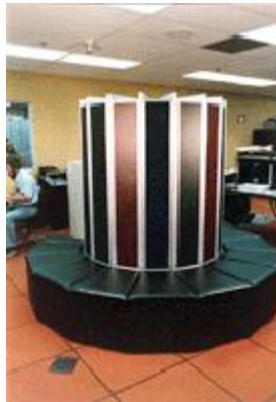
Phase 2: Backward Substitution

Parallel Algorithms

- Coarse-grained algorithms (multi-core CPU)
 - Two-way Gaussian elimination **A set of equations mapped to one thread**
 - Sub-structuring method
- Fine-grained algorithms (many-core GPU)
 - Cyclic Reduction (CR)
 - Parallel Cyclic Reduction (PCR) **A single equation mapped to one thread**
 - Recursive Doubling (RD)
 - Hybrid CR-PCR algorithm

A little history

- Parallel tridiagonal solvers since 1960s:
 - Vector machines: Iliac IV, CDC STAR-100, and Cray-1
 - Message passing architectures: Intel iPSC, and Cray T3E
 - And GPU as well!



Two Applications on GPU



Depth of field blur, Michael Kass et al.

OpenGL and Shader language

Cyclic reduction

2006



Shallow water simulation

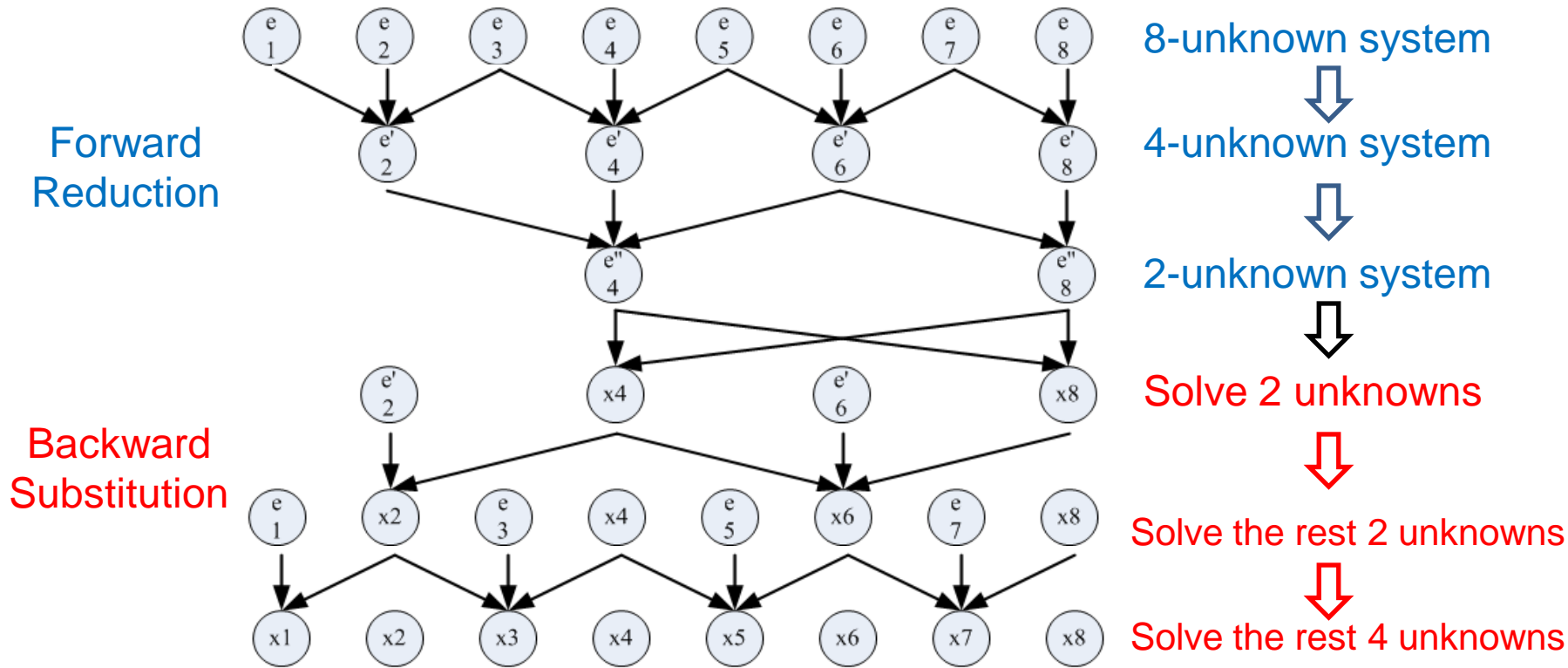
CUDA

Cyclic reduction

2007

Cyclic Reduction (CR)

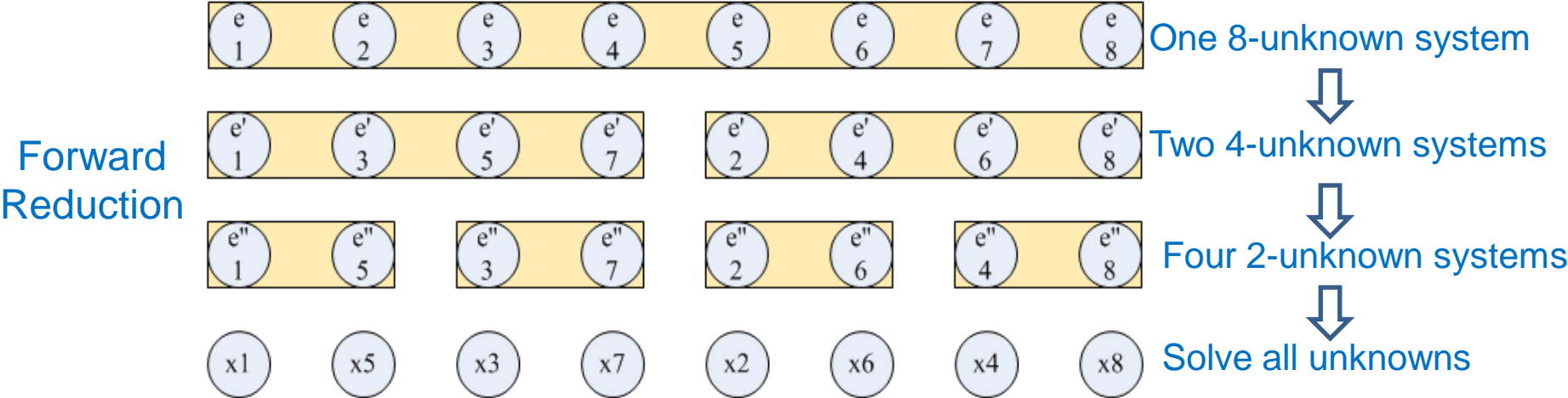
2 threads working



$$2 * \log_2 (8) - 1 = 2 * 3 - 1 = 5 \text{ steps}$$

Parallel Cyclic Reduction (PCR)

4 threads working

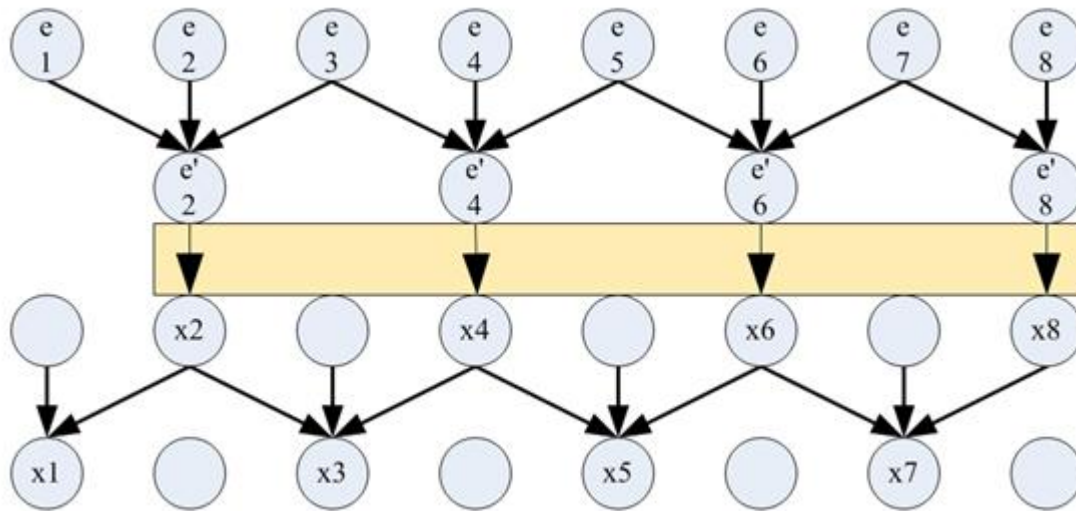


$\log_2(8) = 3$ steps

Hybrid Algorithm (1)

- CR
 - Every step we reduce the system size by half (Good)
 - Some processing cores stay **idle** if the system size is smaller than the number of cores (Bad)
 - Needs more steps to finish (Bad)
- PCR
 - Fewer steps required (Good)
 - Same amount of work for all steps (Bad)

Hybrid Algorithm (2)

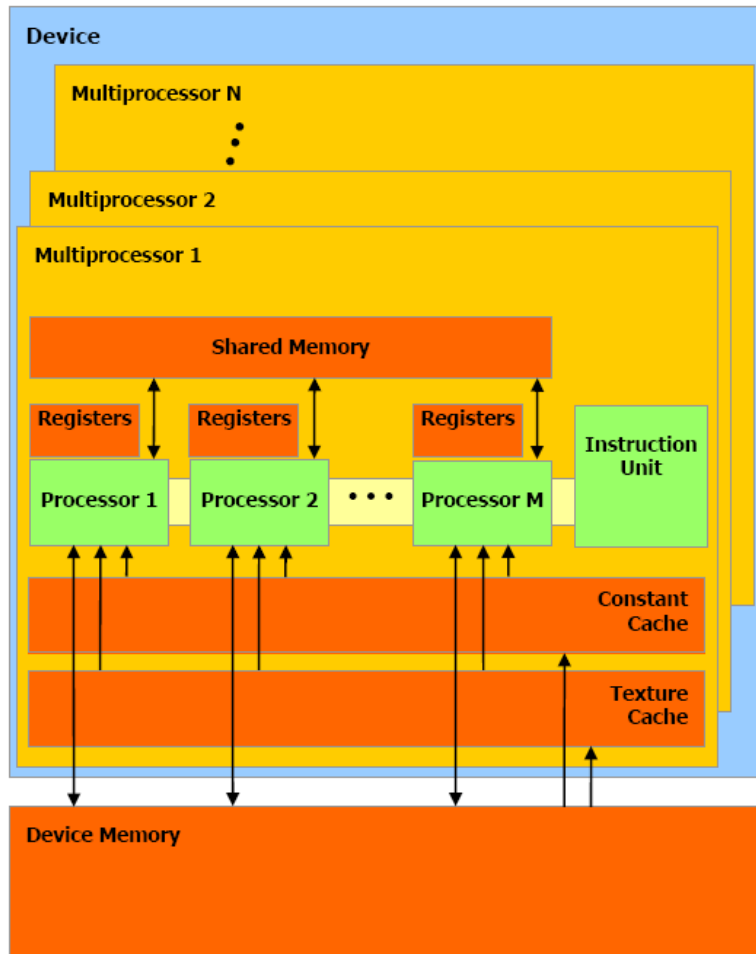


Switch to PCR
Switch back to CR

System size reduced at the beginning
No idle processors
Fewer algorithmic steps

Even more beneficial because of:
bank conflicts
control overhead

GPU Implementation (1)



- Linear systems mapped to multiprocessors (blocks)
- Equations mapped to processors (threads)

GPU Implementation (2)

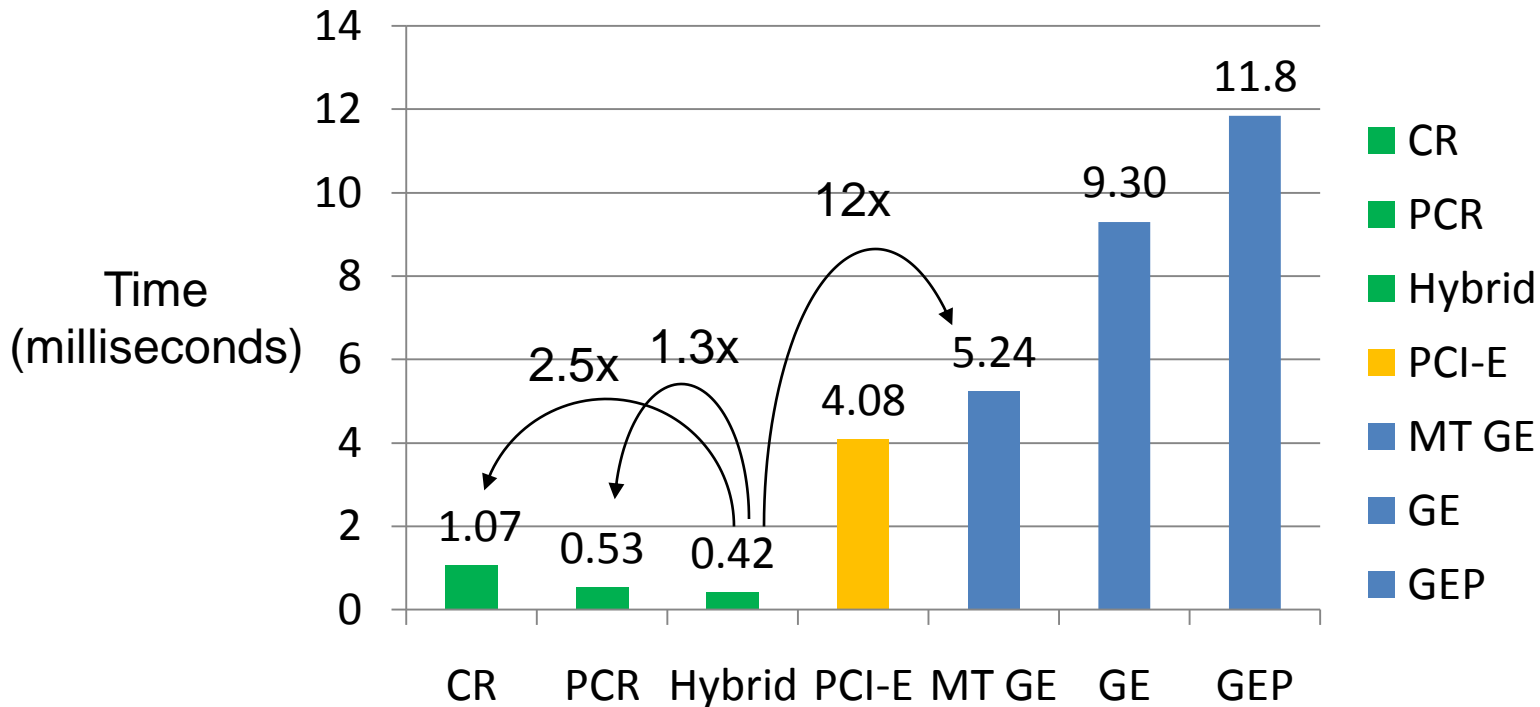
- Storage need: 5 arrays = 3 diagonals + 1 solution vector + 1 right hand side
- All data resides in shared memory if it fits
- Use contiguously ordered threads to avoid unnecessary divergent branches
- In-place data storage
 - Efficient, but introduce bank conflicts to CR

Performance Results – Test Platform

- 2.5 GHz Intel Core 2 Q9300 quad-core CPU
- GTX 280 graphics card with 1 GB video memory
- CUDA 2.0
- CentOS 5 Linux operating system

Performance Results

Solve 512 systems of 512 unknowns



PCI-E: CPU-GPU data transfer

MT GE: multi-threaded CPU Gaussian Elimination

GEP: CPU Gaussian Elimination with pivoting (from LAPACK)

Performance Analysis

- Factors that determine performance
 - Global/shared memory accesses
 - Bank conflicts
 - Computational complexity
 - Overhead for synchronization and loop control

Bottleneck vs. Pie slice



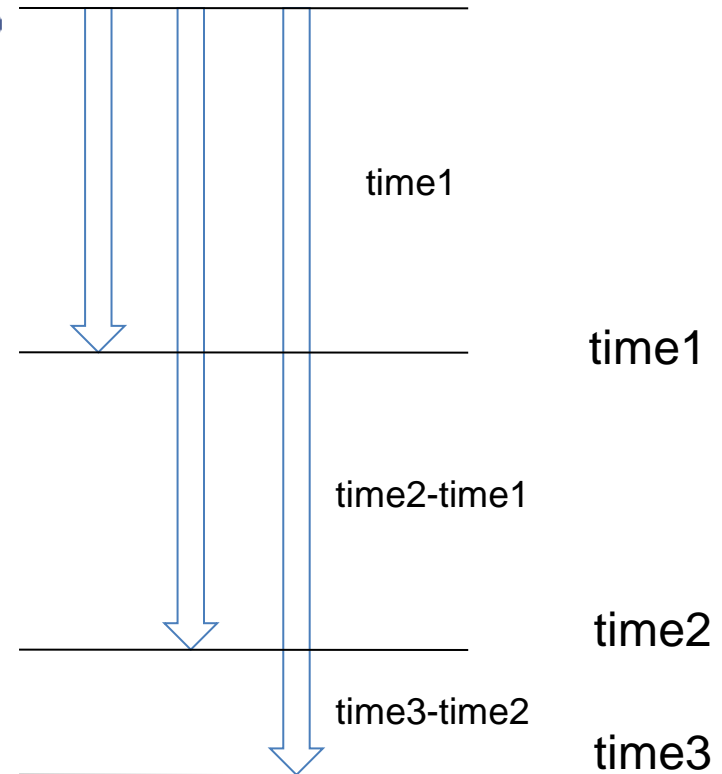
Performance = **min**(factor1, factor2, ...)

Performance = **sum**(factor1, factor2, ...)

Performance Measure

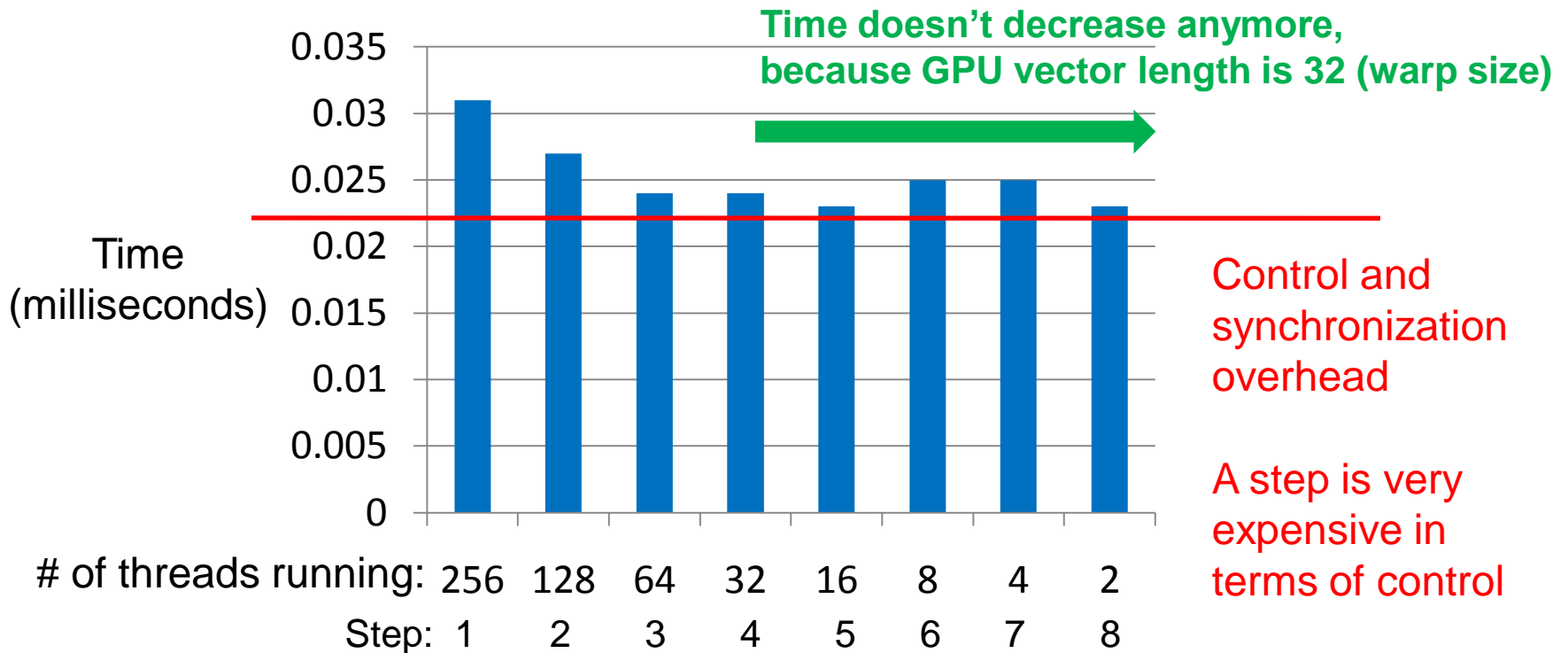
A manual differential method

```
46 __global__ void scan_naive(float *g_odata, float *g_idata, int n)
47 {
48     // Dynamically allocated shared memory for scan kernels
49     extern __shared__ float temp[];
50
51     int thid = threadIdx.x;
52
53     int pout = 0;
54     int pin = 1;
55
56     // Cache the computational window in shared memory
57     temp[pout*n + thid] = (thid > 0) ? g_idata[thid-1] : 0;
58
59     for (int offset = 1; offset < n; offset *= 2)
60     {
61         pout = 1 - pout;
62         pin = 1 - pout;
63         __syncthreads();
64
65         temp[pout*n+thid] = temp[pin*n+thid];
66
67         if (thid >= offset)
68             temp[pout*n+thid] += temp[pin*n+thid - offset];
69     }
70
71     __syncthreads();
72
73     g_odata[thid] = temp[pout*n+thid];
74 }
```



Control Overhead

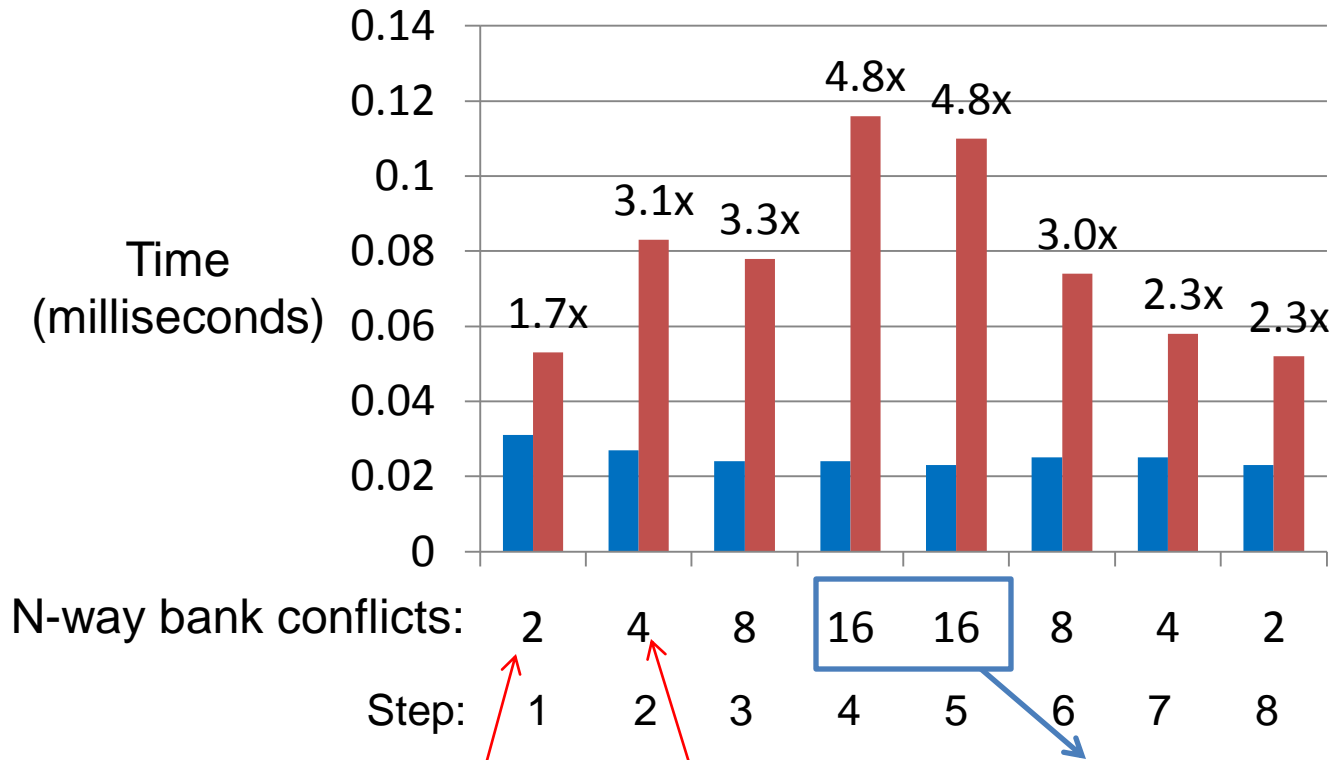
CR: Forward Reduction



Enforce a stride of one to avoid bank conflicts

Bank Conflicts

CR: Forward Reduction



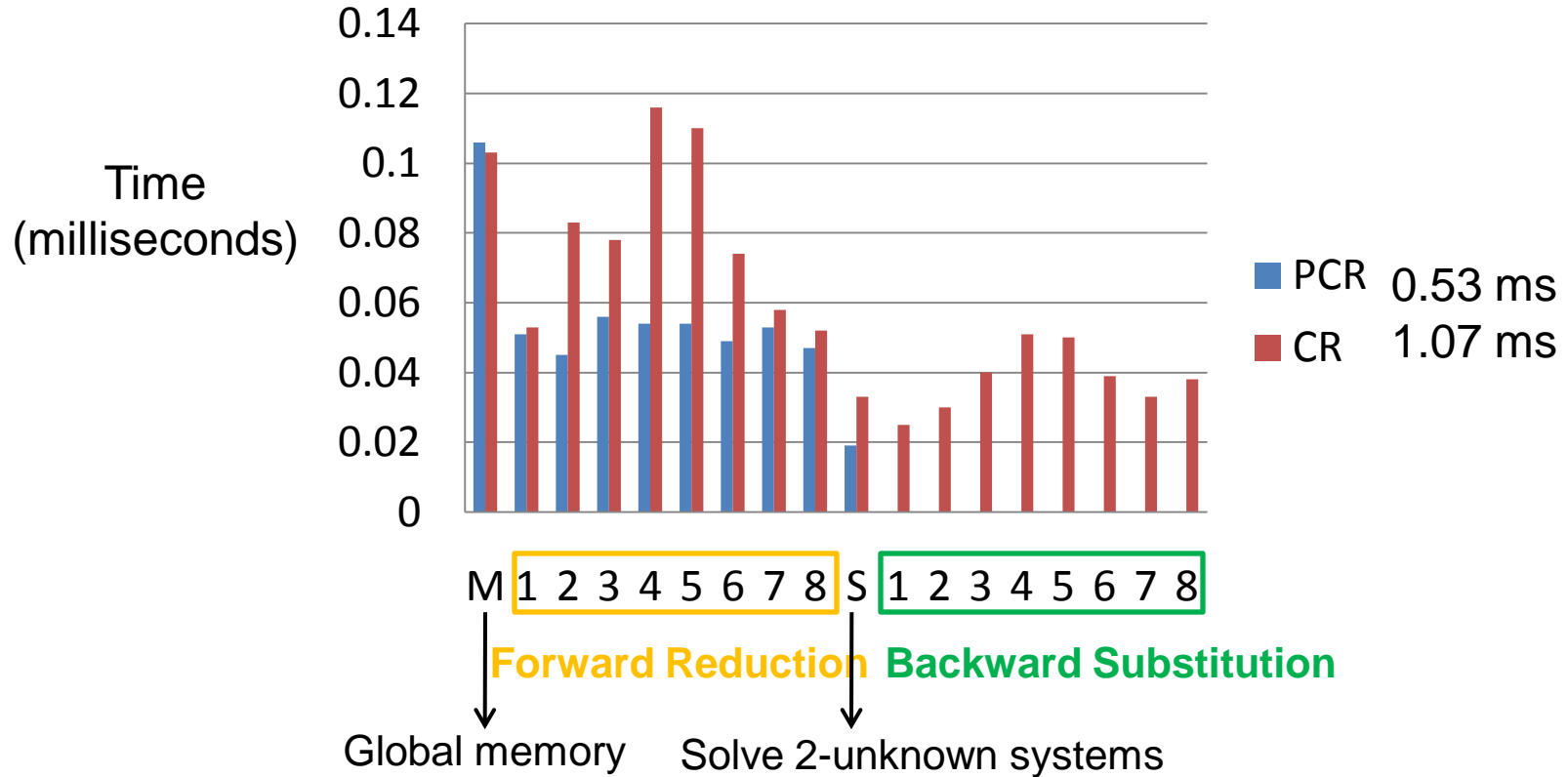
2-way bank conflicts

4-way bank conflicts

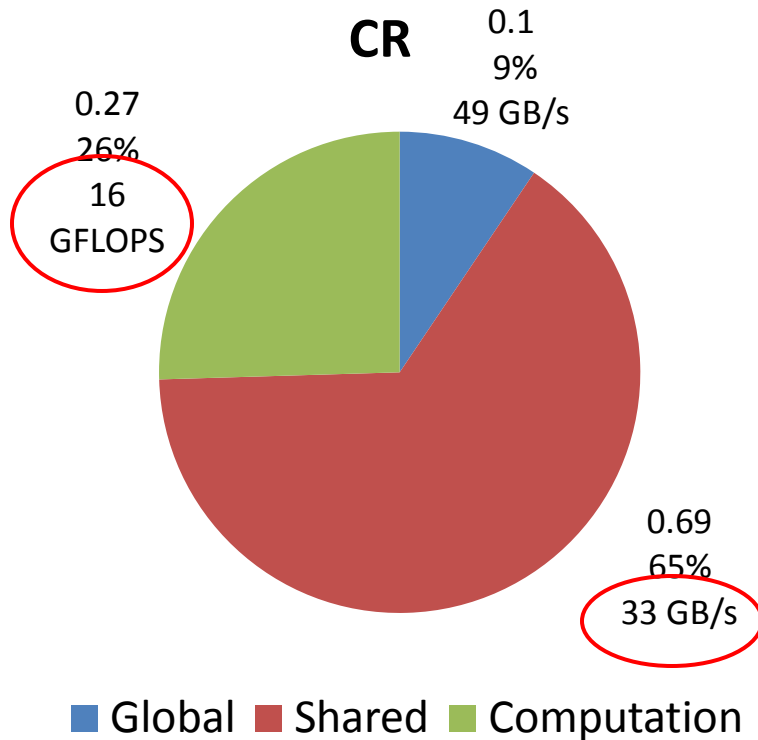
There are 16 banks, so all memory accesses are serialized

CR vs. PCR (1)

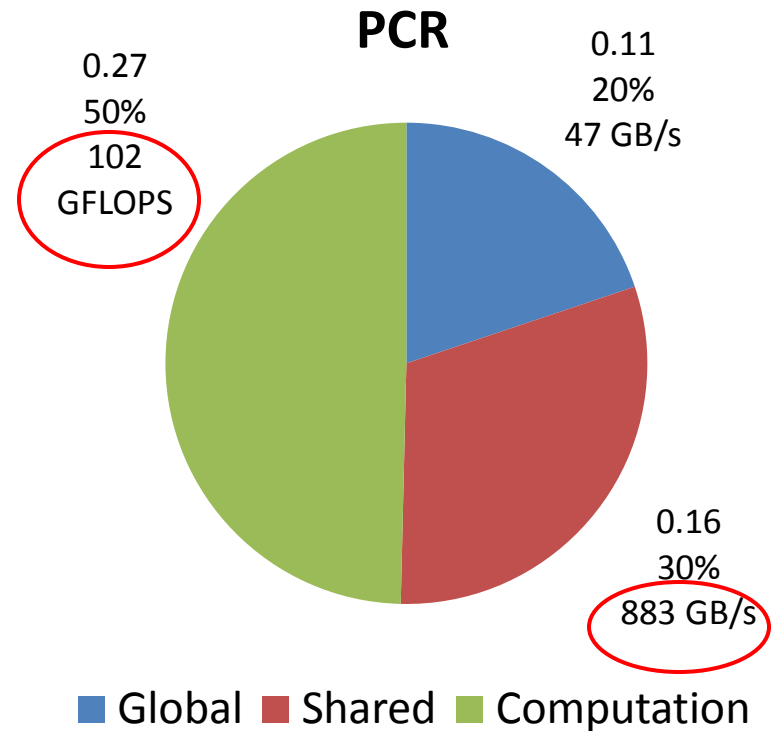
Solve 512 systems of 512 unknowns
(Time Breakdown)



CR vs. PCR (2)



Pros: $O(n)$
Cons: more steps (control overhead), bank conflicts



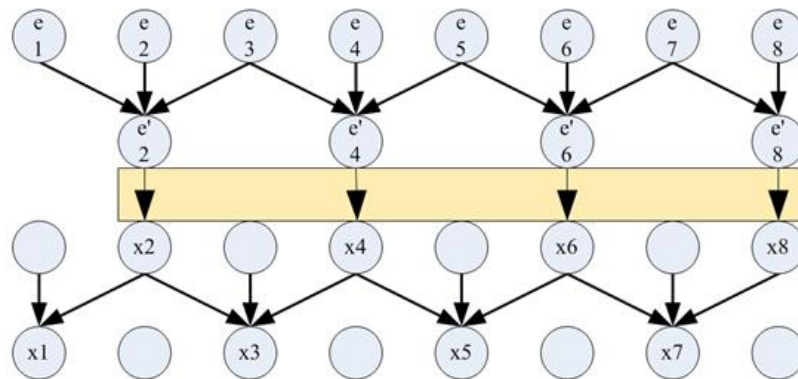
Pros: fewer steps, no bank conflicts
Cons: $O(n \log n)$

Pitfalls

- The higher computation rate and sustained bandwidth, the better
 - They may have different algorithm complexity
- The lower algorithm complexity, the better
 - What if there is considerable amount of control overhead, or bank conflicts, or low hardware utilization

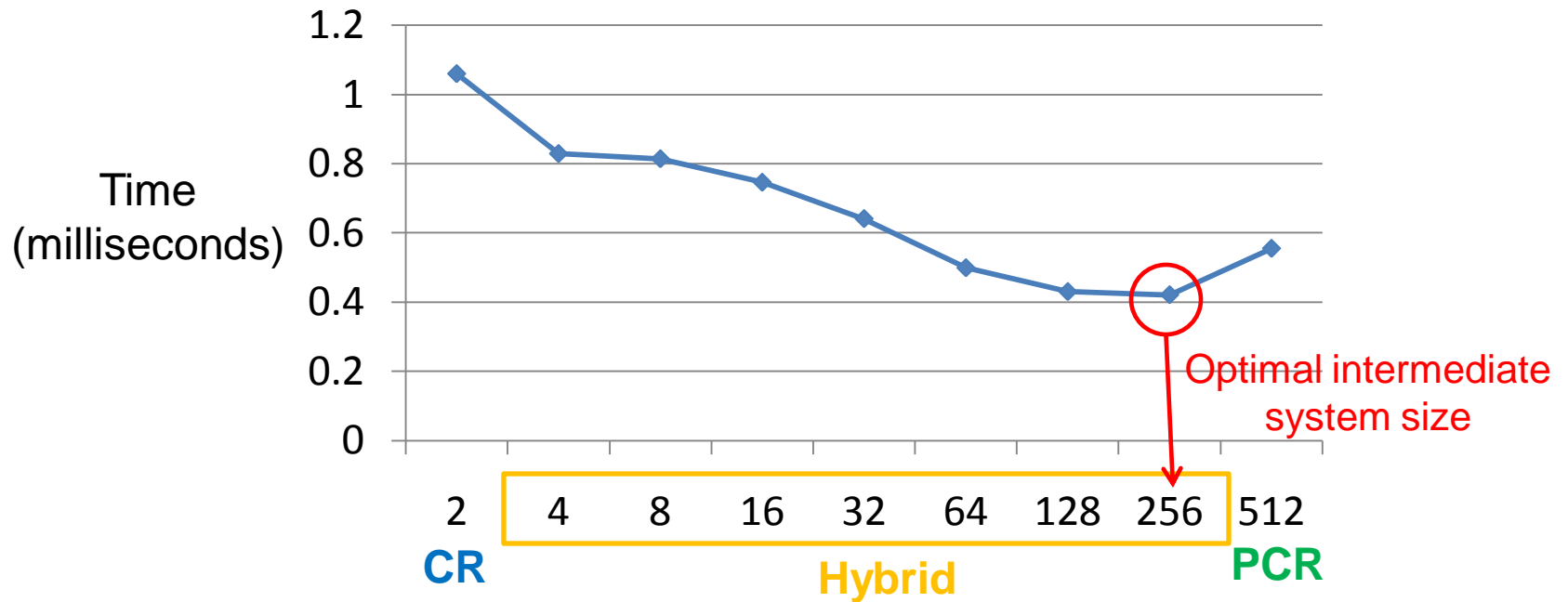
PCR vs Hybrid

- Make tradeoffs between the computation, memory access, and control
 - The earlier you switch from CR to PCR
 - The fewer bank conflicts, the fewer algorithmic steps
 - But more work



Hybrid Solver – Sweet Point

Optimal performance of hybrid solver
Solving 512 systems of 512 unknowns



Known issues and future research

- PCI-E data transfer
- Double precision
- Pivoting
- Block tridiagonal systems
- Handle large systems that cannot fit into shared memory
- Automatic performance profiling

Summary

- We studied the performance of 3 parallel solvers on GPU
- We learned two major lessons
 - Component-based rather than bottleneck-based
 - » Performance is more complicated than either compute-bound or memory-bound
 - We can make tradeoffs between these components, and we need to make the right tradeoff

Questions?

Thanks