

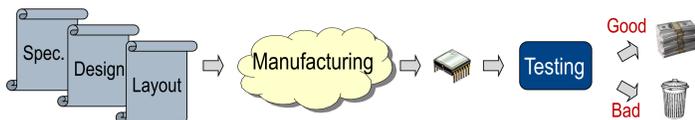
Introduction

With the advance of integrated circuit (IC) manufacturing technology, the geometry of transistors and their associated interconnect continue to decrease thus allowing greater levels of integration within a single chip. The increased circuit complexity that results however brings new challenges to IC testing, whose objective is to clearly identify chips that do not operate exactly as desired. It is essential to reduce overall test and die-scrap cost while maintaining quality as technology progresses. Achieving this objective requires the understanding of the tradeoffs among design, manufacturing, and test.

In this work, GPUs are utilized to reduce the overall test and die-scrap cost. A generalized test methodology is developed to create high-quality tests capable of detecting modern defects encountered in the IC manufacturing process. The parallelization inherent to the methodology is exploited to reduce the test development and execution cost through the use of CUDA.

VLSI Testing

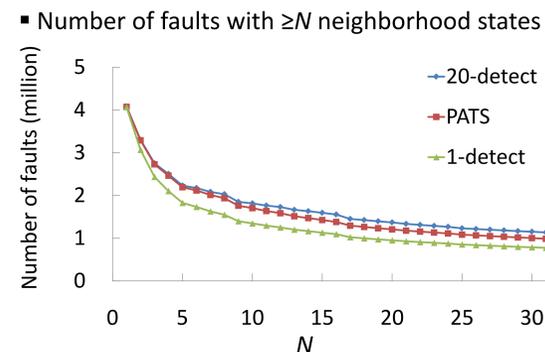
The objective of VLSI testing is to screen out failing parts caused by defects in the manufacturing process. Defect behaviors are modeled as faults, which serve as the targets for test generation. The stuck-at fault model, which assumes that a single signal line in a faulty circuit is permanently fixed to either logic 0 or 1, has been widely used as the basis of test generation and evaluation because of its low cost and low complexity. The stuck-at fault model alone, however, is not sufficient to detect the new, emerging defect types now encountered in advanced manufacturing processes.



To improve test quality, physically-aware N -detect test, which considers physical design (i.e., layout) information, was proposed. In physically-aware N -detect test, the objective is to detect each stuck-at fault N times with N different "states" (i.e., set of logical values) for the lines that are physically close to the targeted fault. It is expected that by exploring conditions that are more likely to activate and detect arbitrary, unmodeled defects, the defect detection characteristics of the test can be improved, which in turn reduces die-scrap cost.

Physically-Aware N -Detect Test Selection

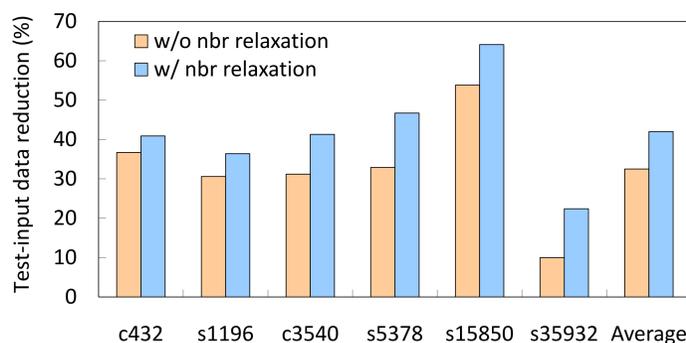
A physically-aware test selection (PATS) software has been developed to generate a compact, neighborhood-based, N -detect test set by greedily selecting the most effective tests from a large test pool. The objective of PATS software is to maximize state coverage for a user-provided, test-set size constraint. PATS has been used to generate a physically-aware 10-detect test set for an in-production IBM ASIC. The DPPM reduction due to PATS would be approximately 30. This number is not trivial for an in-production ASIC fabricated with mature processes.



Physically-Aware N -Detect Test Relaxation

The applicability of a physically-aware N -detect test set can be further improved by employing test relaxation. The benefit of performing test relaxation comes from the flexibility of reassigning the unspecified test inputs for (1) test compression, (2) reducing power incurred during scan test, (3) embedding tests to detect a targeted fault more times, and (4) enriching tests to target other fault types. Experiment results demonstrate that the physically-aware N -detect test relaxation (PATR) procedure reduces, on average, 40% of the test-input data while preserving the physically-aware N -detect fault coverage.

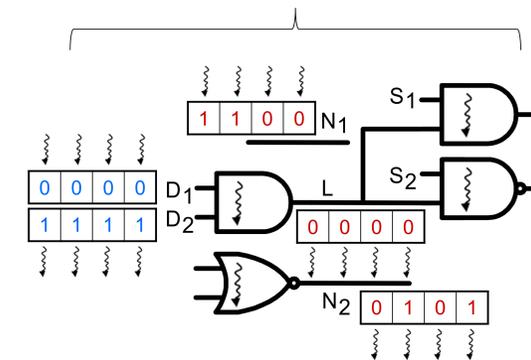
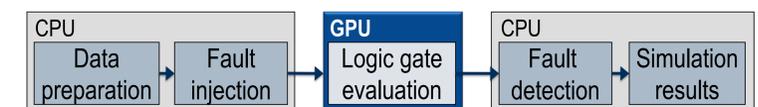
Percentage of test-input data reduction for benchmark circuits



Cost Reduction through Utilization of GPUs

Both physically-aware N -detect test selection and test relaxation rely on fault simulation to determine the fault detection status. The runtime of the two procedures therefore depends on the time for performing fault simulation, which is the bottleneck in our current implementation. It has been demonstrated that the runtime for fault simulation can be significantly reduced by utilizing GPUs and the CUDA environment. Moreover, in test relaxation, tests can be relaxed concurrently to achieve even higher speedup. The efficiency of our test methodology can therefore be enhanced by exploiting the parallelism inherent in the physically-aware N -detect test selection and relaxation procedures.

Parallelized fault simulation for physically-aware N -detect test selection and relaxation



Summary

Defect behaviors continue to become more complicated as design and manufacturing technology advance. A systematic and effective test methodology is needed to detect defective parts in wafer sort and reduce die-scrap cost. We have developed a cost-effective physically-aware N -detect test methodology that includes a test selection and a test relaxation procedure. Via silicon experiments, physically-aware N -detect test has been demonstrated to improve defect detection for modern designs by exploiting defect locality. We believe the quality of test resulting from our test methodology can be further improved while simultaneously reducing cost through the use of CUDA.