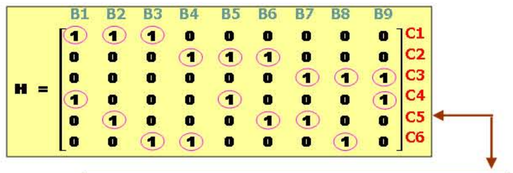
Noise Adaptive LDPC decoding using Particle filtering based on parallel GPU architecture

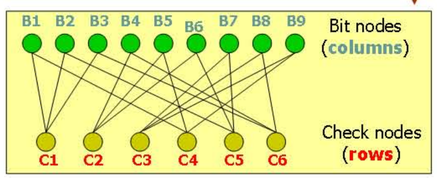
Shuang Wang, Lijuan Cui, Samuel Cheng and Robert C. Huck
School of Electrical and Computer Engineering
University of Oklahoma

Low-Density Parity-Check (LDPC) Codes

Parity check matrix : sparse matrix

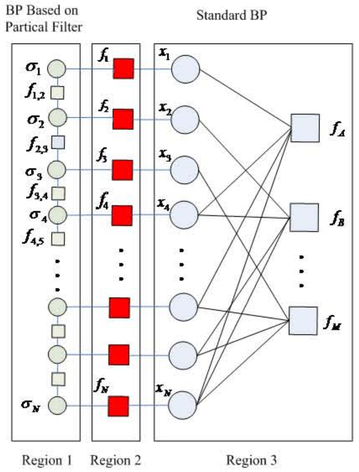


Tanner graph

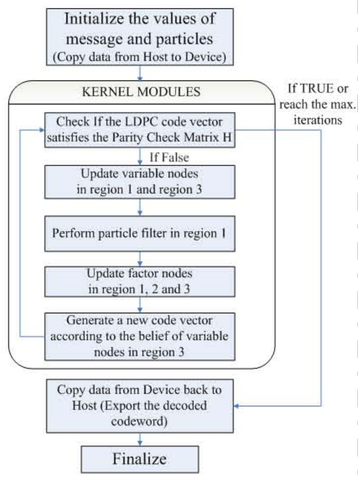


$$X = (x_1, x_2, \ldots x_N) \qquad H \cdot X^T = 0$$

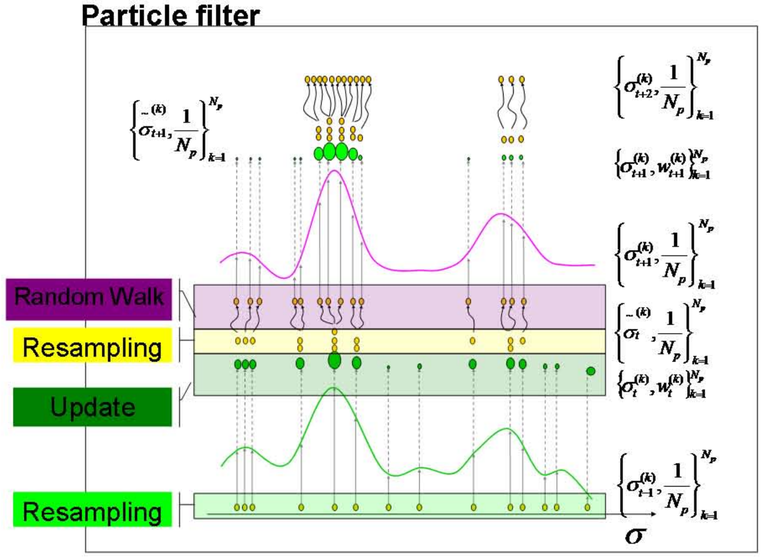
Factor graph of BP based on PF

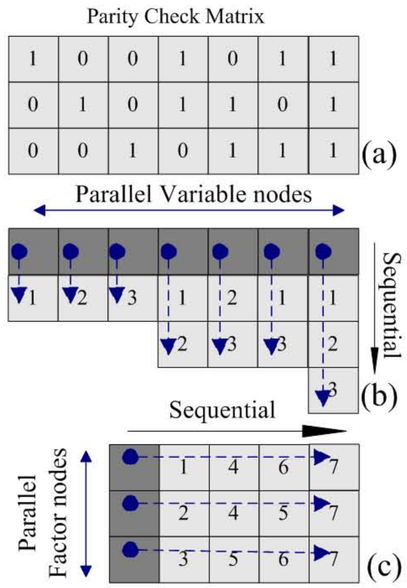


Workflows of our Algorithm

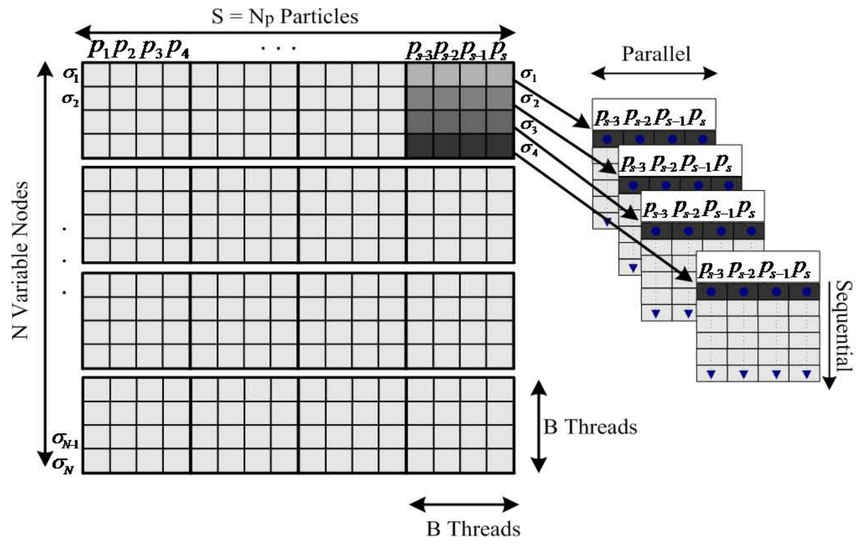


Particle filter

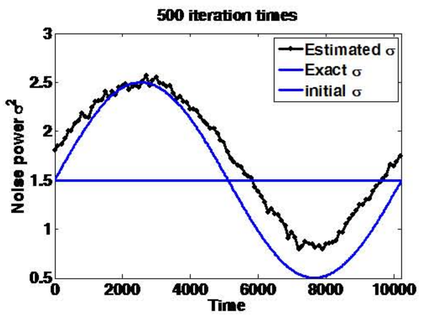




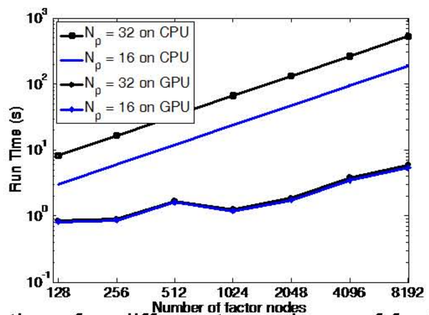
Schematic figures of a computational block for region 3.



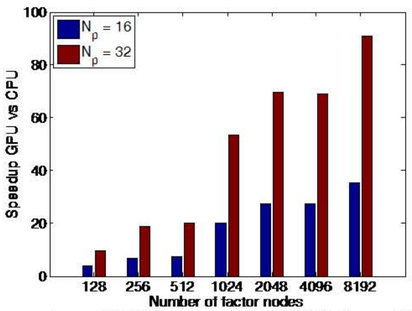
The grid of thread blocks that update variable nodes in region 1 and a schematic figure of Computational Tile, where p_i is one of particles and σ_i is one of variable nodes.



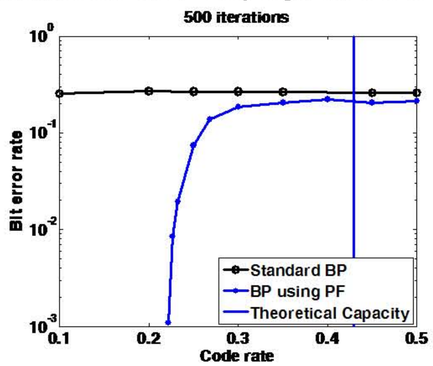
Estimation of noise power for sinusoidal time-varying AWGN channel



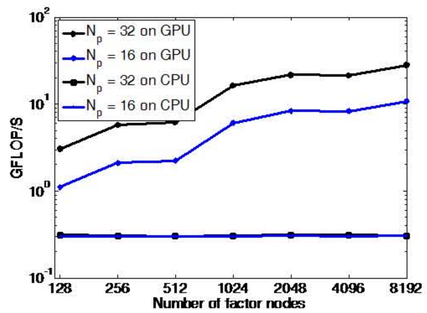
Run time for different numbers of factor nodes with 16 and 32 particles.



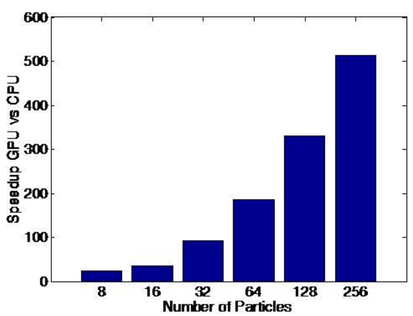
Speedup GPU versus CPU for different numbers of factor nodes



Error probability for LDPC codes over a sinusoidal time-varying AWGN channel



Performance for different numbers of factor nodes with 16 and 32 particles.



Speedup GPU versus CPU for different numbers of particles, where the size of parity check matrix is 8192 by 16384,